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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,637	01/20/2004	Chantal Auricchio	854063.737	8266

38106 7590 05/02/2005

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,637	AURICCHIO ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 8-10* is/are rejected.

7)☒ Claim(s) *4-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/280/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Gupta et al (5,247,478).

Gupta shows:

1. A nonvolatile switch comprising:

an input terminal (0, Fig. 3);

an output terminal (source of transistor 82 connected to gate 55);

a selection terminal (WORD LINE);

a first (BL1) and a second biasing terminal (GND);

a memory element of flash type (72), having a first conduction region (drain) connected to said first biasing terminal and a second conduction region (source) connected to said second biasing terminal;

a pass transistor(82), having a first conduction region (drain) connected to said input terminal and a second conduction region (source) connected to said output terminal; and

a pair of common-gate regions, having a common floating gate region (92) and a common control gate region (WORD LINE), which are capacitively coupled together,

said memory element and said pass transistor sharing said common-gate regions, and said common control-gate region being connected to said selection terminal.

2. The switch according to claim 1, further comprising a second pass transistor (84), having a first conduction region connected to an own input terminal (I) and a second conduction region connected an own output terminal (source), said second pass transistor, said memory element and said pass transistor sharing said common-gate regions (WORD LINE).

The apparatus described above is applicable to the method claim 9.

The limitations of claim 8 are rejected as above, furthermore, a first, a second, and a third biasing generator are word line driver, bit-line driver, and ground generating circuit.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3, 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Sansbury et al (6,456,529).

Sansbury shows:

1. A nonvolatile switch comprising:

an input terminal (drain R1, Fig. 4);

an output terminal (source R1);

a selection terminal (CG1);

a first (BL) and a second biasing terminal (SL);

a memory element of flash type (one on the left side), having a first conduction region (drain) connected to said first biasing terminal and a second conduction region (source) connected to said second biasing terminal;

a pass transistor(R1), having a first conduction region (drain) connected to said input terminal and a second conduction region (source) connected to said output terminal; and

a pair of common-gate regions, having a common floating gate region (251, Fig. 2A) and a common control gate region (248), which are capacitively coupled together, said memory element and said pass transistor sharing said common-gate regions, and said common control-gate region being connected to said selection terminal.

3. The switch according to claim 1 wherein said common gate regions extend parallel to one another on top of said body of semiconductor material (col. 6, lines 11-14).

8. The limitations of claim 8 are rejected as above, furthermore, a first, a second, and a third biasing generator are CG driver, bit-line driver, and SL driver circuit.

9. The apparatus described above is applicable to the method claim 9.

10. The control method according to claim 9 wherein said step of program biasing comprises:

applying a first and a second potential, respectively, to a first and a second conduction region of said memory element, and applying a third potential to said common control gate region of said memory element and of said pass transistor in a writing step (col. 7, lines 11-27);

leaving said first conduction region of said memory element floating, applying a fourth potential to said second conduction region of said memory element, and applying a fifth potential to said common control gate region of said memory element and of said pass transistor in an erasing step (col. 8, lines 48-56); and

leaving said first conduction region of said memory element floating, applying a reference potential to said second conduction region of said memory element, applying a sixth potential to said common control gate region of said memory element and said pass transistor, and detecting possible data on an output terminal of said pass transistor (inherent limitation, since this is normal operation after programming).

Allowable Subject Matter

4. Claims 4-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

4/26/05